# An Evolutionary Meta-Heuristic For State Justification Insequential Automatic Test Pattern Generation

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**Neural Networks, 2001. Proceedings. IJCNN '01. International Joint conference;Publication Date: 2001;Vol: 1,On page(s): 767-772 vol.1;ISBN: 0-7803-7044-9**

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## Summary

Sequential circuit test generation using deterministic, fault-oriented algorithms is highly complex and time consuming. New approaches are needed to enhance the existing techniques, both the reduce execution time and improve fault coverage. Evolutionary algorithms have been effective in solving many search and optimization problems. A common search operation in sequential ATPG is to justify a desired state assignment on the sequential elements. State justification using deterministic algorithms is a difficult problem and is prone to many backtracks, which can lead to high execution times. In this work, we propose a hybrid approach which uses a combination of evolutionary and deterministic algorithms for state justification. A new method based on Genetic Algorithms is proposed, in which we engineer state justification sequences vector by vector. This is in contrast to previous approaches where GA is applied to the whole sequence. The proposed method is compared with previous GA-based approaches. Significant improvements have been obtained for ISCAS benchmark circuits in terms of state coverage and CPU time. Furthermore, it is demonstrated that the state-justification sequence generated, helps the ATPG in detecting a large number of hard-to-detect faults